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Research article

Performance & Reliability Analysis for VLSI Circuits Using Cadence Virtuoso @ 45 nm Technology

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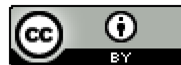

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ABSTRACT:

The objective of this research paper is on finding out the reliability of an inverter circuit and two CMOS gate, a combination of two inverters connected with an RC model as an interconnect structure using cadence virtuoso tool at gpdk 45 nm technology. Reliability in terms of electronic circuit basically depends on hot-carrier injection, negative biasing temperature instability, positive biasing temperature instability and slightly due to the effect of time-dependent gate oxide breakdown. The inverter used here is without any load effect at output terminal and then applying capacitive load at output terminal. Reliability analysis is done by comparing power, delay and output voltage after certain interval of time [1]. **Copyright © AJESTR, all rights reserved.**

Keywords: HCI, NBTI, PBTI, TDDB.

Introduction:

Performance and reliability is a key issue in defining the operation of the transistors and circuit over the prolonged period. Bias temperature instability is one of the most challenging issues in circuit reliability. There are generally four terms which play vital role in defining the reliability of transistors as HCI, NBTI, PBTI and TDDB effecting performance, noise margin, leakage current, delay between input-output voltages and reliability in terms of aging.

These terms are mainly responsible for the performance and reliability degradation of any circuit. All the above mentioned four terms are described below. First these phenomenons are shown on transistors effecting on drain current and inverted channel and then inverter with applied input voltage, I_{DP} and I_{DN} [1].

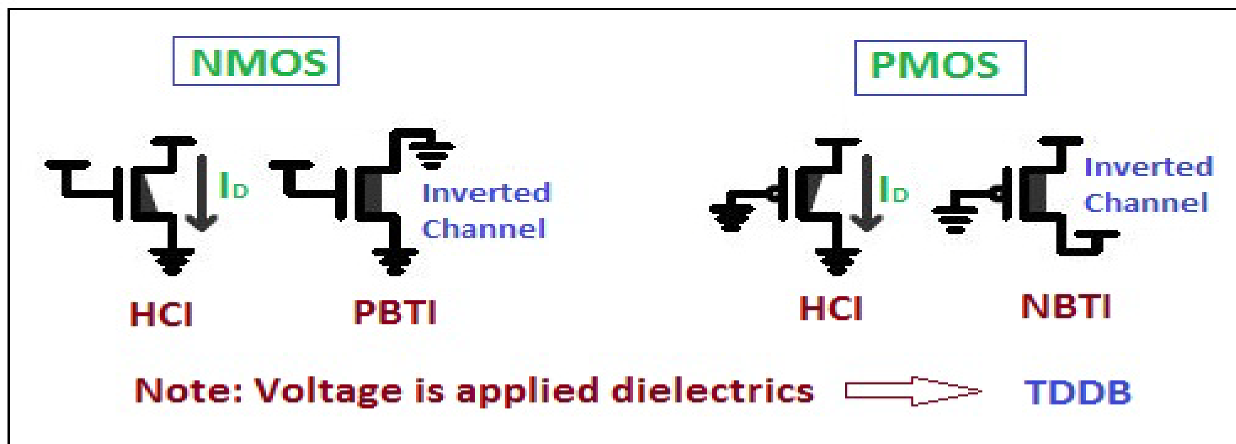

Fig.1. Schematic of an inverter.

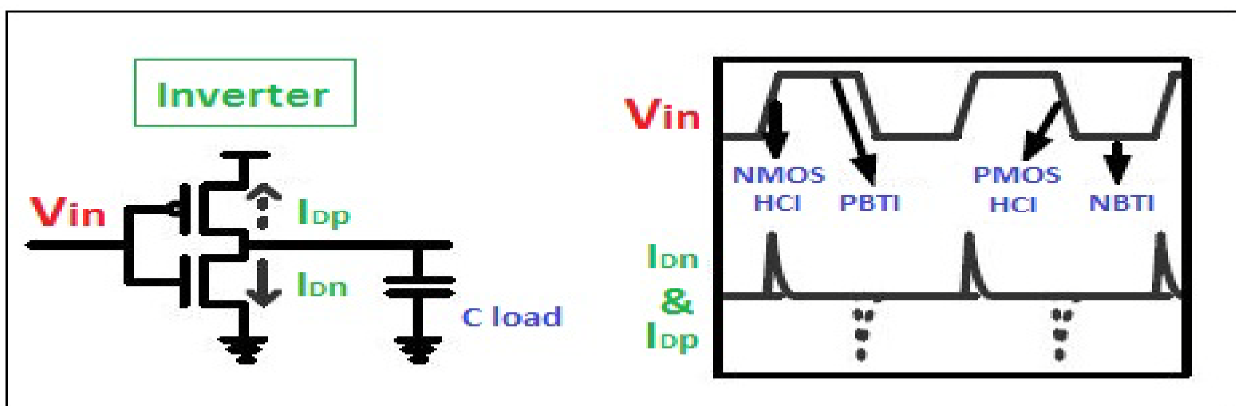

Fig.2. Schematic of an inverter.

HCI: It is basically one of the mechanisms that severely affect the reliability of semiconductors of solid-state devices. HCI manifests itself for an increase in the value of the threshold voltage and secondary degradation of the carrier mobility, especially for the NMOS transistors. The degradation takes place when a device is generally biased in strong inversion with a large V_{DS}. It is a strong voltage dependence factor [2].

NBTI: NBTI in PMOS transistor is recognized as the major reliability concern in advanced CMOS process technologies. This mechanism is recognized by a positive shift in the absolute value of the PMOS V_{th}. It occurs when a device is biased in strong inversion without large V_{DS}.

It is a key reliability concern in MOSFETs. NBTI plays a vital role to manifests as an increase in the V_{th} and consequent fall in value of I_D and G_m of a MOSFET, especially for the PMOS transistors. It is of valid concern for devices operating in p-channel, since they almost operate with negative gate-to-source voltage [3].

PBTI: It is a critical circuit reliability issue in highly scaled CMOS technologies. It is generally concerned for NMOS transistors in highly scaled CMOS technology and becomes a serious degrading factor in high-k metal gate technology [4].

TDDB: It is generally a failure mechanism in MOSFETs, when the gate oxide breaks down for the result of long time application concerning low electric field. It is commonly used test for constant stress. Cu interconnects are greatly affected and vulnerable to failure due to time-dependent gate oxide breakdown of low-k die-electrics. Main concern is that the life time decreases with increased porosity. In addition to these issues, the HCI, NBTI and PBTI effects will further degrade the margin and can eventually lead to reduced I_D, reduced speed, shift in threshold voltage, degradation in transconductance or mobility, generation of unwanted current components and circuit failures over prolonged periods [5].

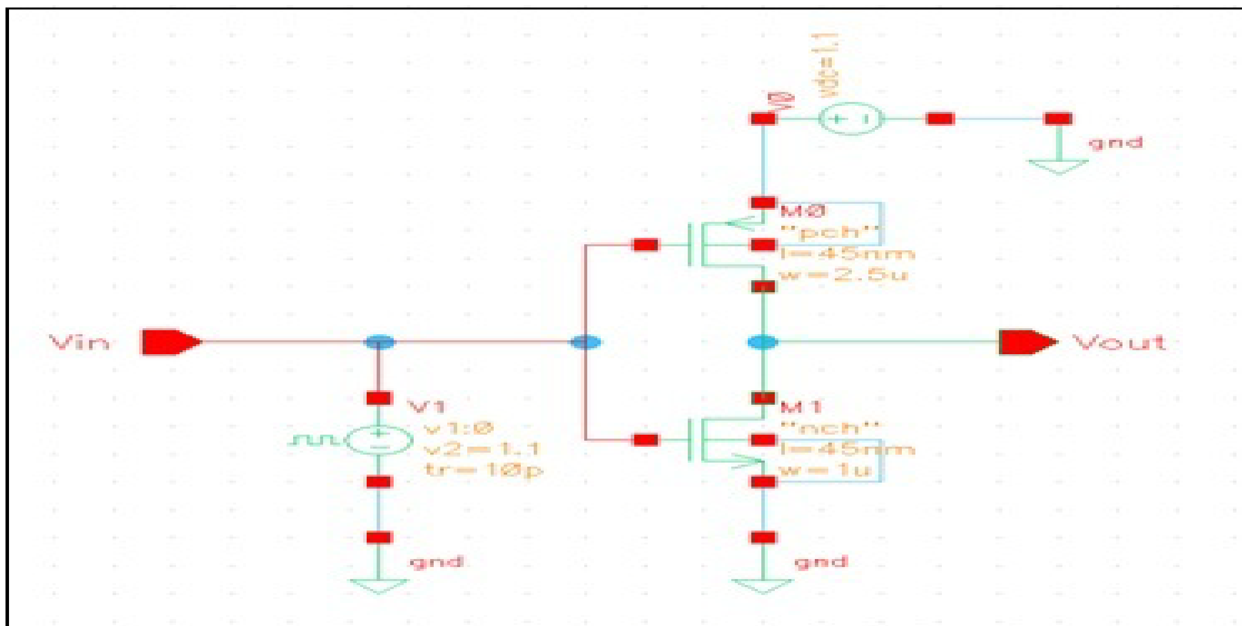

Fig.3. Schematic of an inverter.

Above figure shows the schematic of an inverter circuit designed with a PMOS of width 2.5 um and length 45 nm and an NMOS width 1 um and length 45 nm, using pch and nch model libraries respectively. The input is applied using a pulsating signal of 1.1 V, rise time of 10 ps, fall time 10 ps, pulse width 10 ns and period of 20 ns respectively. The circuit is operated with V_{DC} 1.1 V using BSIM4 model files addresses the MOSFET physical effects into sub-100 nm regime for 40 ns [1].

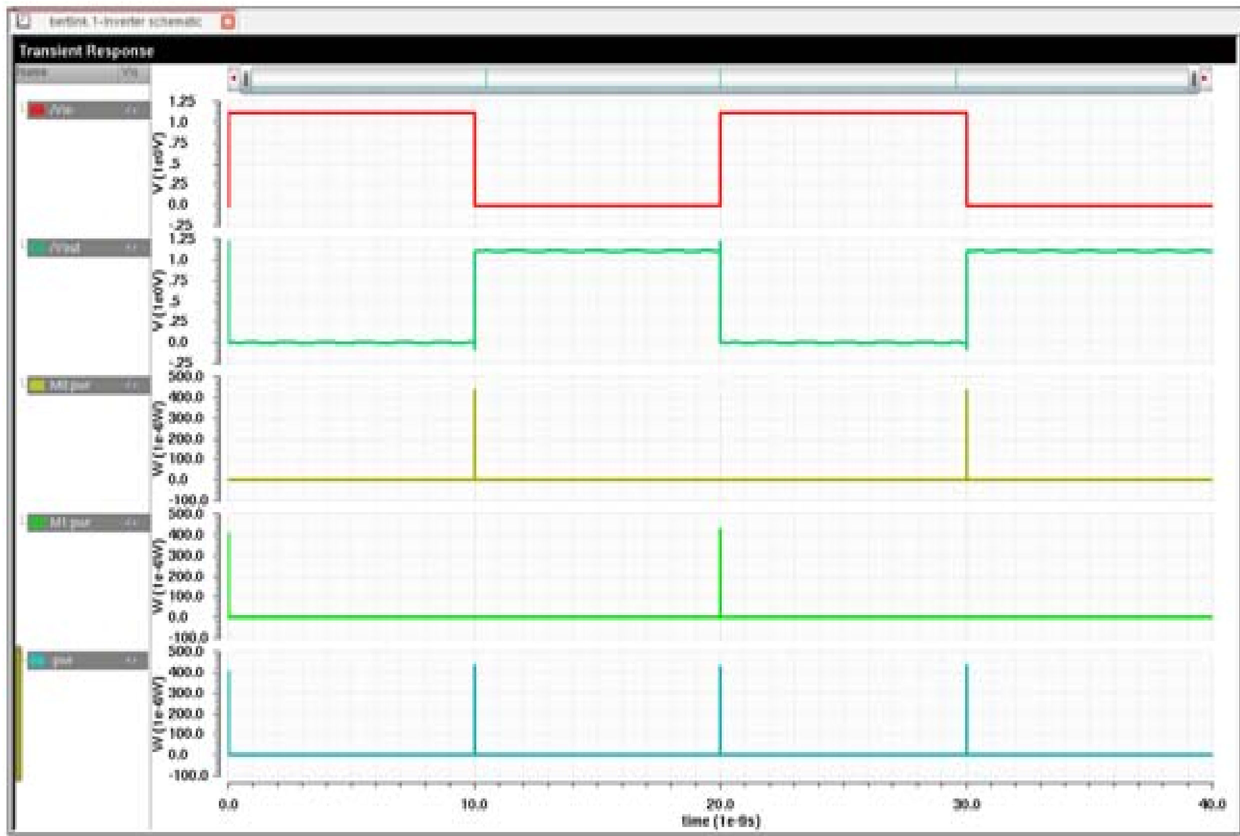

Fig.4. Transient response of an inverter (Vin, Vout, Power of PMOS, Power of NMOS & Power of the Inverter).

Table-1. Values obtained in transient analysis of inverter for duration of 0 to 40 ns.

Max Power of Inverter	432.9E-6 W	Max Value of Vin	1.1 V
Min Power of Inverter	49.09E-12 W	Min Value of Vin	0 V
Avg Power of Inverter	185.6E-9 W	Avg Value of Vin	550.6E-3 V
Max Value of Vout	1.226 V	Max Power of PMOS	427E-6 W
Min Value of Vout	-105.2 E-3 V	Min Power of PMOS	48.33E-18 W
Avg Value of Vout	549.5E-3 V	Max Power of NMOS	432.9E-6
Delay B/w Vin & Vout	11.18E-12 s	Min Power of NMOS	2.12E-18

Further DC analysis is done and the corresponding values of Vin, Vout and power is calculated. DC analysis is done from -5 V to 5V.

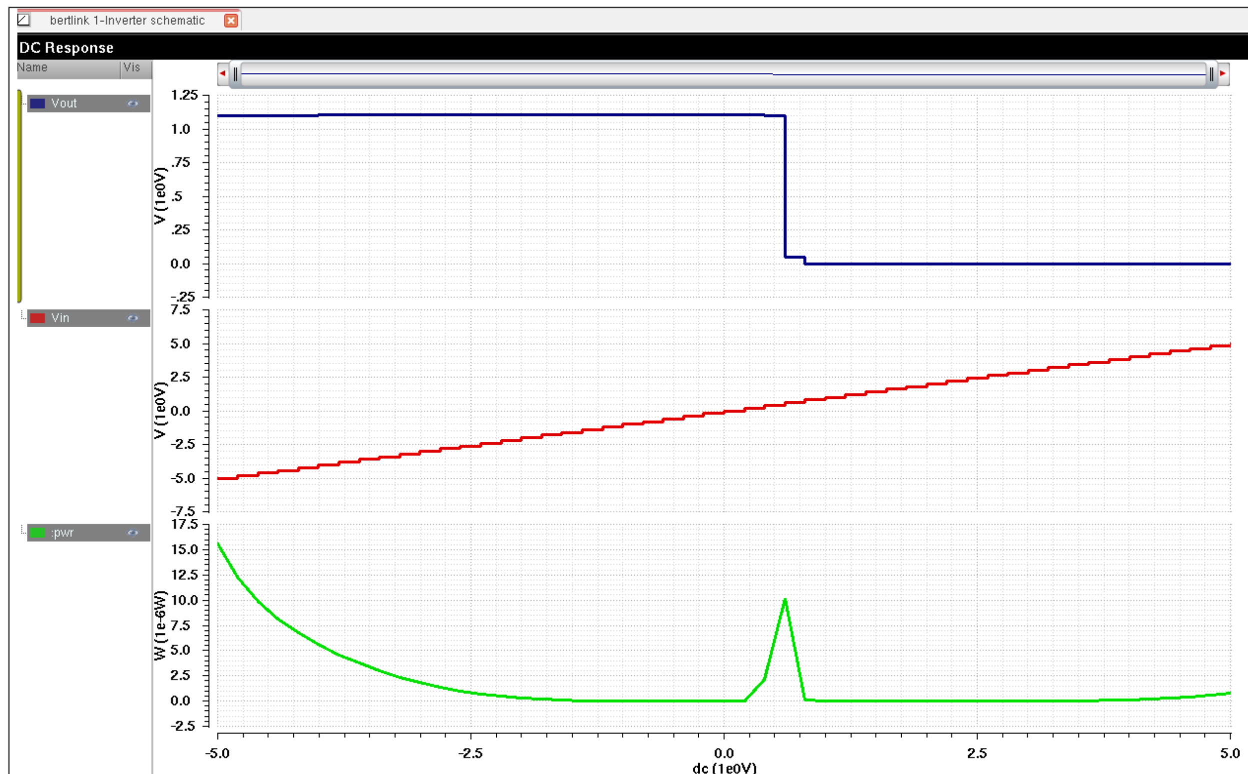

Fig.5. DC response of inverter (Vout, Vin & Power of the Inverter).

Table-2. Values obtained @ DC analysis of inverter from -5 V to 5 V.

Max Value of Vin	+5 V	Min Value of Vout	42.02E-9 V
Min Value of Vin	-5 V	Max Value of Power	15.54E-6 W
Max Value of Vout	1.1 V	Min Value of Power	17.96E-12 W

Inverter is also tested for noise performance at 5 GHz frequency and amplitude of 10 dBm from input to output values. The result obtained is very much significant and acceptable since the noise reduces drastically as the inverter starts operating and continues.

For the analysis of noise ports are added at both terminals and capacitor is placed. The figure below shows the schematic diagram of the inverter designed for noise analysis. The value of capacitor used is mentioned below. Three capacitors are used, one at the input terminal and two at output terminal are added. Input Capacitor (C_0) is of 10 fF in series with port -0, Output Capacitor (C_1) is of 10 fF and Output Capacitor (C_2) is of 500 fF in parallel with the port-1.

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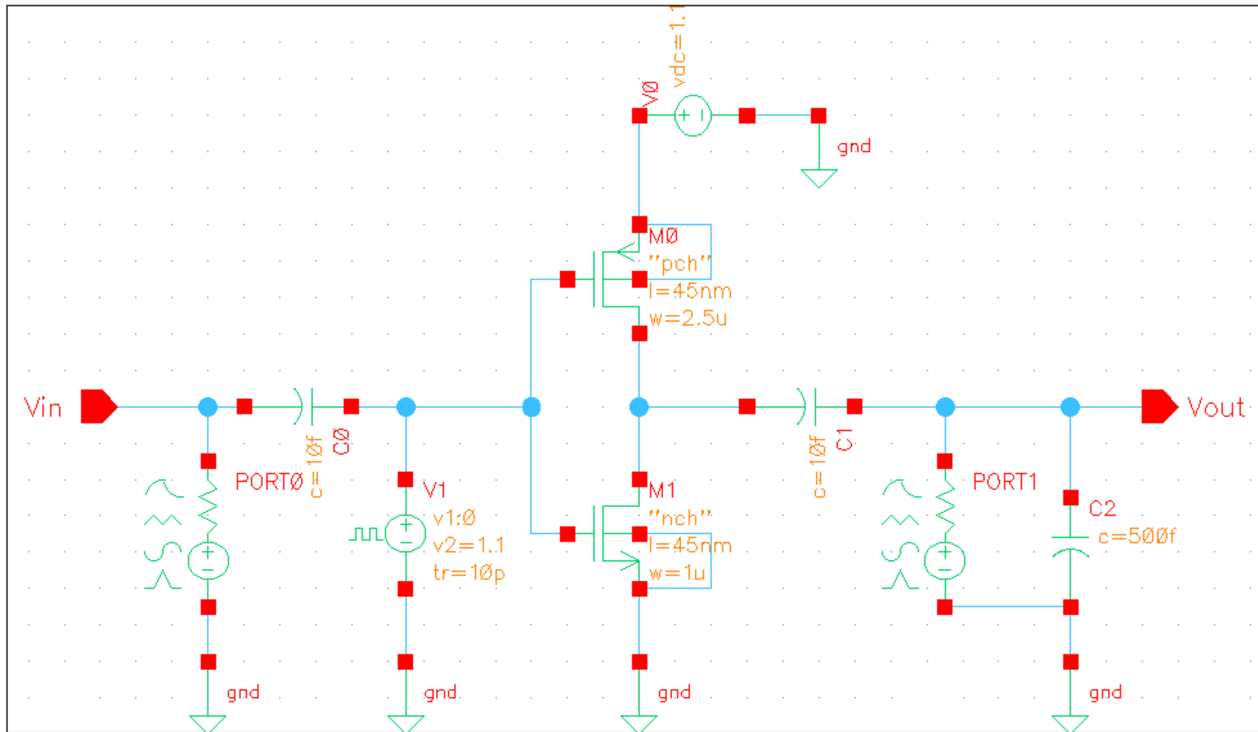

Fig.6. Schematic of inverter for noise analysis using ports at both terminals @ 5 GHz.

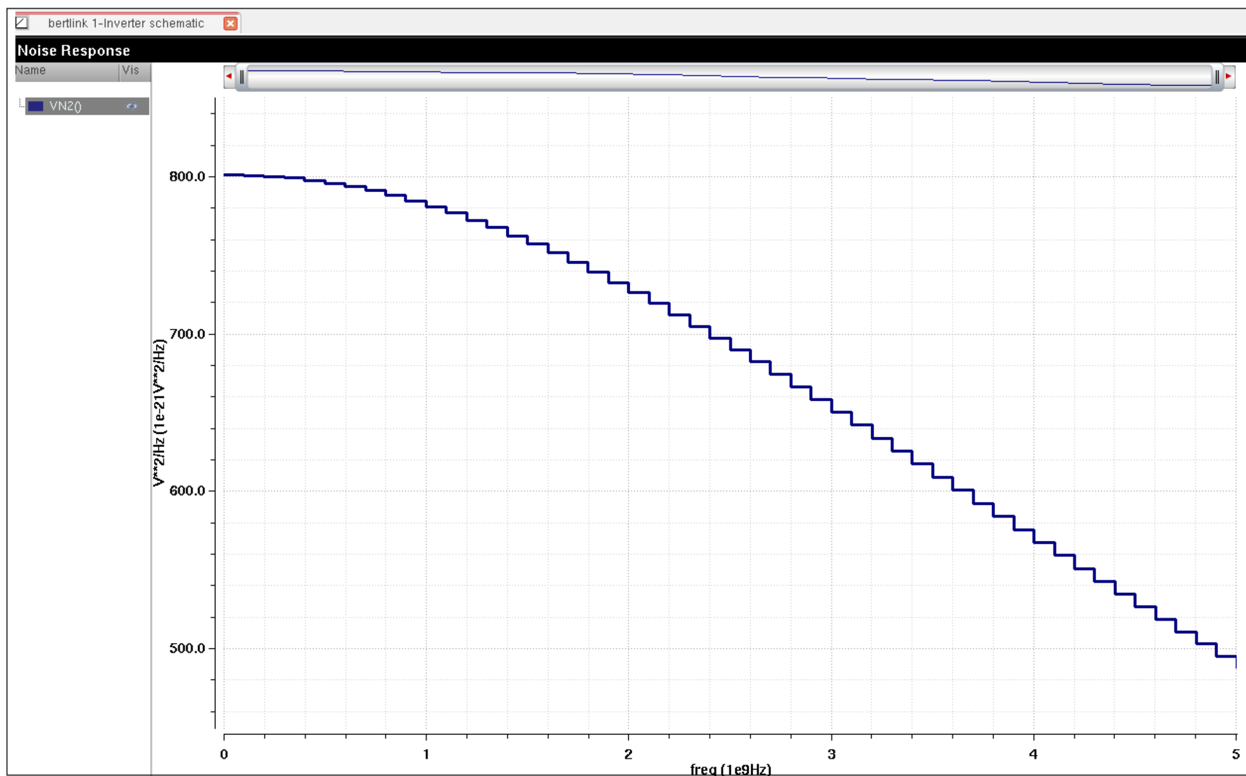

Fig.7. Noise response of inverter @ 5 GHz.

Reliability Analysis of Inverter In Terms of Average Power:

In the conventional sense, the reliability of a system is defined as the probability that it will perform its required function under stated conditions, for a stated period of time. The reliability of inverter is analyzed at five different time intervals. The major problem is that the impact of HCI degradation on circuit performance. It is generally observed that under static DC stress condition, HCI device degradation for both NMOS and PMOS transistors produces changes in the threshold voltage, transconductance and current-driving capability. It is noted that when the transistors are under the dynamic operating conditions of a CMOS circuit, the MOSFET terminal voltage varies with respect to time. For this we need to model I_D as a function of time.

Average power delivered falls w.r.t time period, due to the effects of HCI, NBTI, PBTI & TDDB and circuit failures occurs over prolonged periods [6].

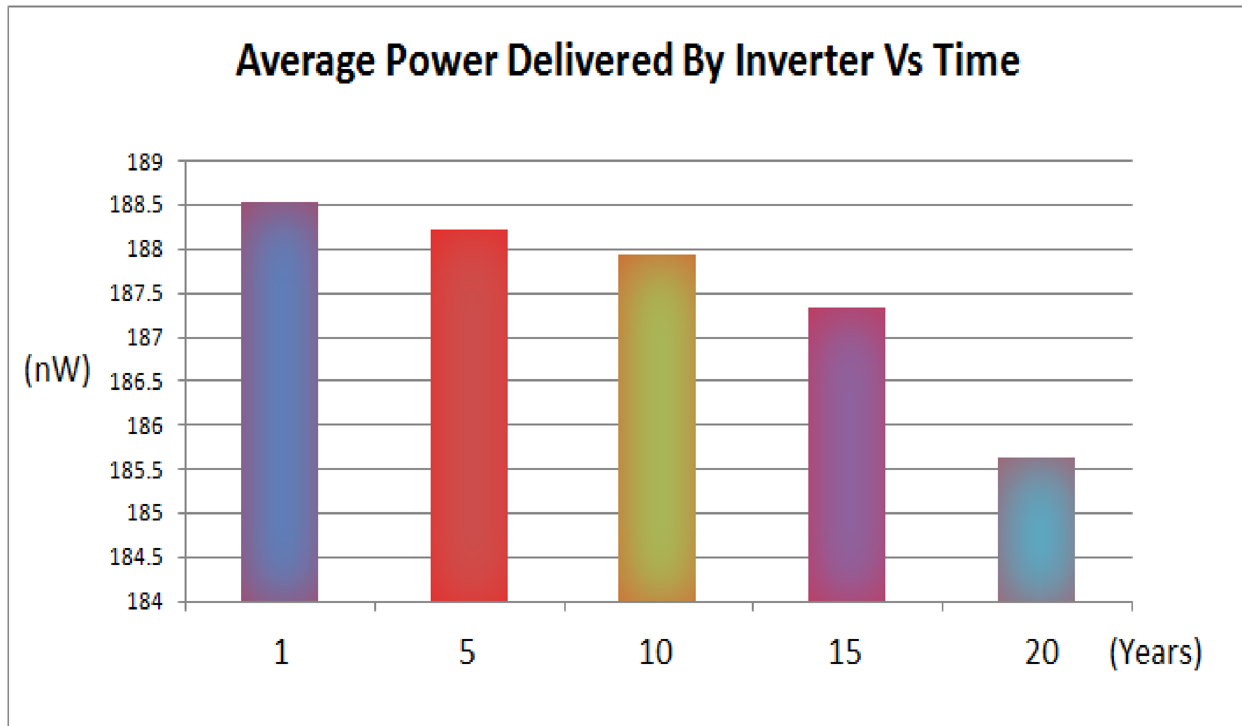

Fig.8. Reliability analysis for inverter in terms of average power delivered vs. time.

Now to compare the effect of electrical interconnects we analyze the case of two CMOS gate (a combination of two inverters joined through an RC model). The schematic below shown depicts two CMOS gate.

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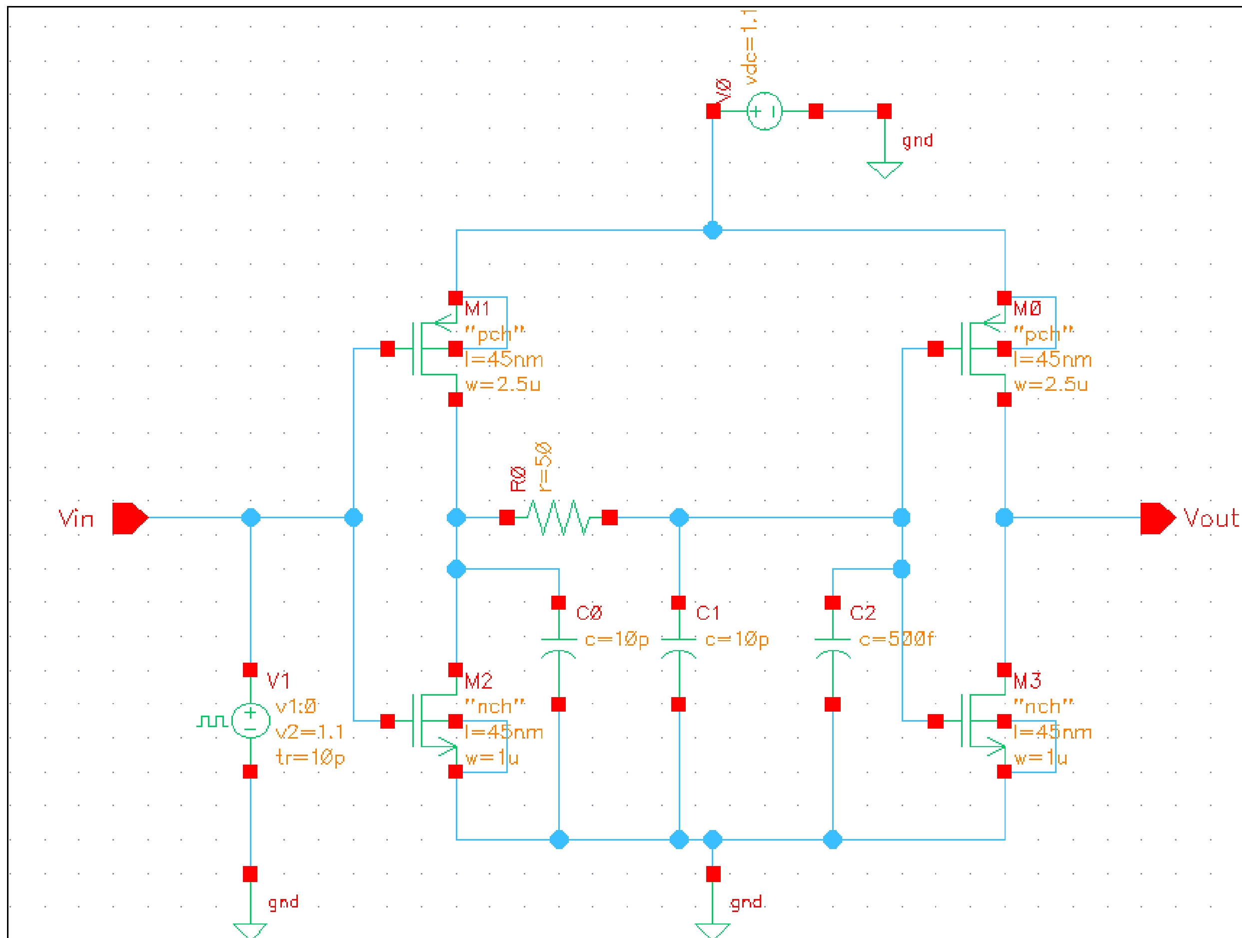

Fig.9. Schematic of two CMOS gate.

Above figure shows the schematic of two CMOS gate circuit designed with two PMOS of width 2.5 um and length 45 nm and two NMOS width 1 um and length 45 nm, using pch and nch model libraries respectively. The input is applied using a pulsating signal of 1.1 V, rise time of 10 ps, fall time 10 ps, pulse width 10 ns and period of 20 ns respectively. The circuit is operated with V_{DC} 1.1 V using BSIM4 model files addresses the MOSFET physical effects into sub-100 nm regime for 40 ns. The electrical interconnection between the inverter is composed of an RC model [7].

Table-3. Values of passive components used in two CMOS gate schematic.

R_0	50 Ohm	**C_0**	1 pF
C_1	1 pF	**C_2**	5 fF

The transient analysis is analyzed for 100 ns, and Vin Vs Vout is calculated.

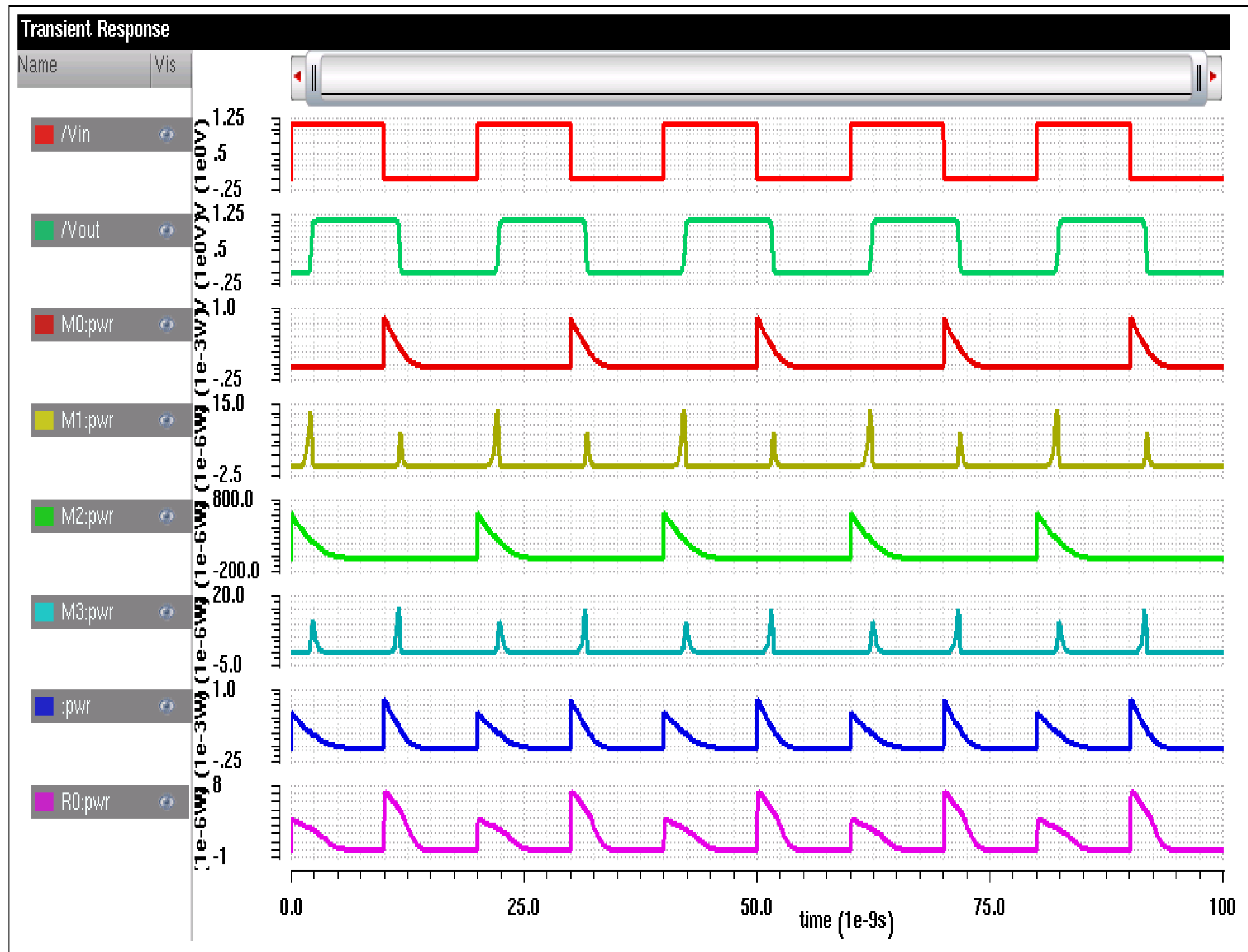

Fig.10. Transient response of two CMOS gate (Vin, Vout, power consumed by Mo, M1, M2, M3, Power of the circuit & power consumed by of resistance).

Table-4. Values obtained in transient analysis of two CMOS gate for duration of 0 to 100 ns.

Max Value of Vin	1.1 V	Min Power of PMOS-1	12.09E-18 W
Min Value of Vin	0 V	Max Power of NMOS-1	13.24E-6 W
Avg Value of Vin	550.6E-3 V	Min Power of NMOS-1	333.4E-18 W
Max Value of Vout	1.1 V	Max Power of PMOS-2	610.1E-6 W
Min Value of Vout	-149.4E-6 V	Min Power of PMOS-2	449.9E-18 W
Avg Value of Vout	519.5E-3 V	Max Power of NMOS-2	15.9E-6 W
Max Power of Circuit	837.6E-6 W	Min Power of NMOS-2	2.454E-18 W
Min Power of Circuit	114.0E-12 W	Max Power of R0	7.150E-6
Avg Power of Circuit	123.3E-6 W	Min Power of R0	469.2E-21 W
Max Power of PMOS-1	837.5E-6 W		

Further DC analysis is done and the corresponding values of Vin, Vout and power is calculated. DC analysis is analysed in the range from -5 V to 5V.

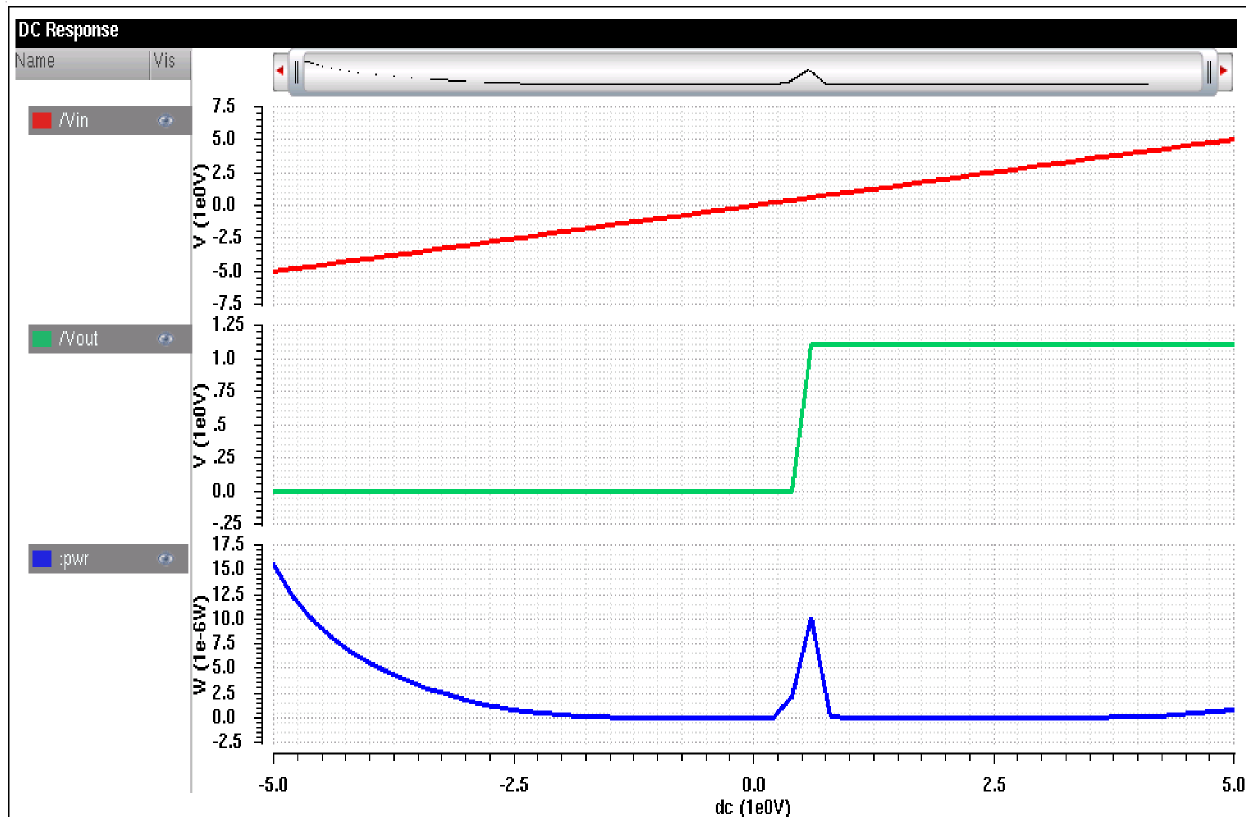

Fig.11. DC response of two CMOS gate (Vin, Vout & Power of the circuit).

Table-5. Values obtained @ DC analysis of two CMOS gate from -5 V to 5 V.

Max Value of Vin	+5 V	Max Value of Power	15.54E-6 W
Min Value of Vin	-5 V	Min Value of Power	82.91E-12 W
Max Value of Vout	1.1 V	Avg Value of Power	1.704E-6 W
Min Value of Vout	40.80E-9 V		

Two CMOS gate is also tested for noise performance at 5 GHz frequency and amplitude of 10 dBm from input to output values. The result obtained is very much significant and acceptable since the noise reduces drastically as the inverter starts operating and continues. The figure below shows the schematic diagram of two CMOS gate using ports at both terminals designed for noise analysis. Three capacitors are used, one at the input terminal and two at output terminal are added. Input Capacitor (C_0) is of 1 pF in series with port -0, Output Capacitor (C_1) is of 1 fF and Output Capacitor (C_2) is of 500 fF in parallel with the port-1.

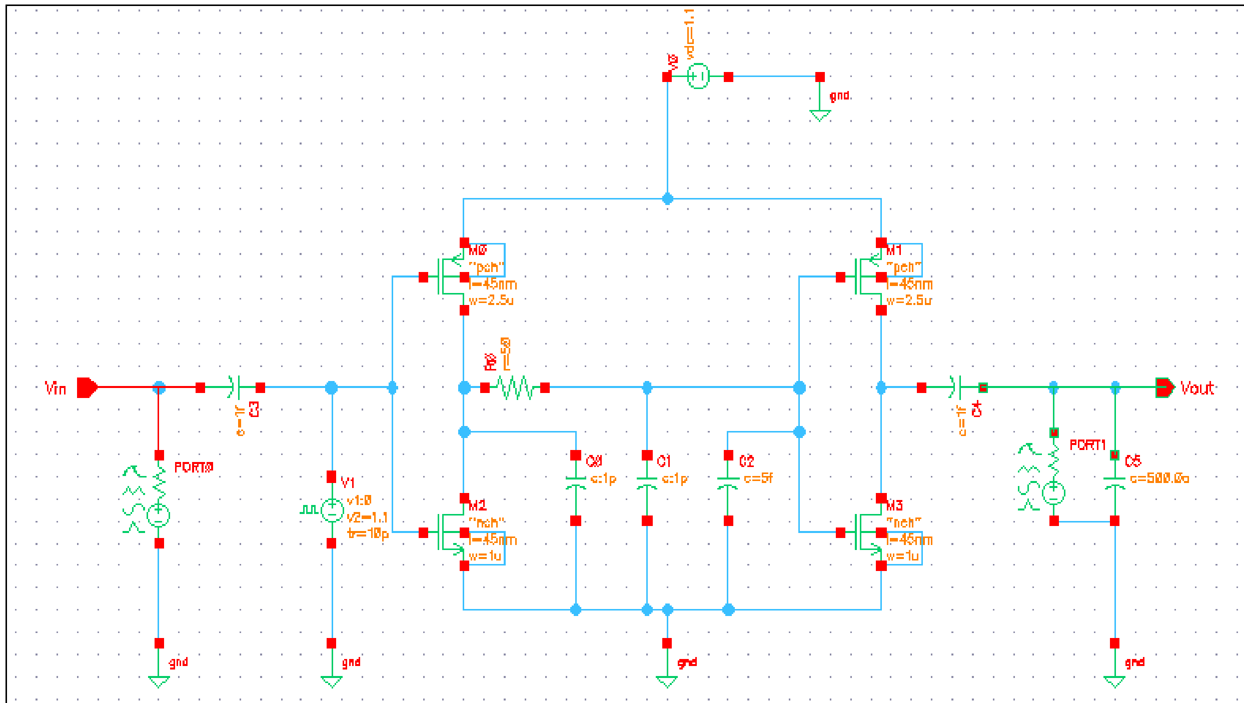

Fig.12. Schematic of two CMOS gate for noise analysis using ports at both terminals @ 5 GHz.

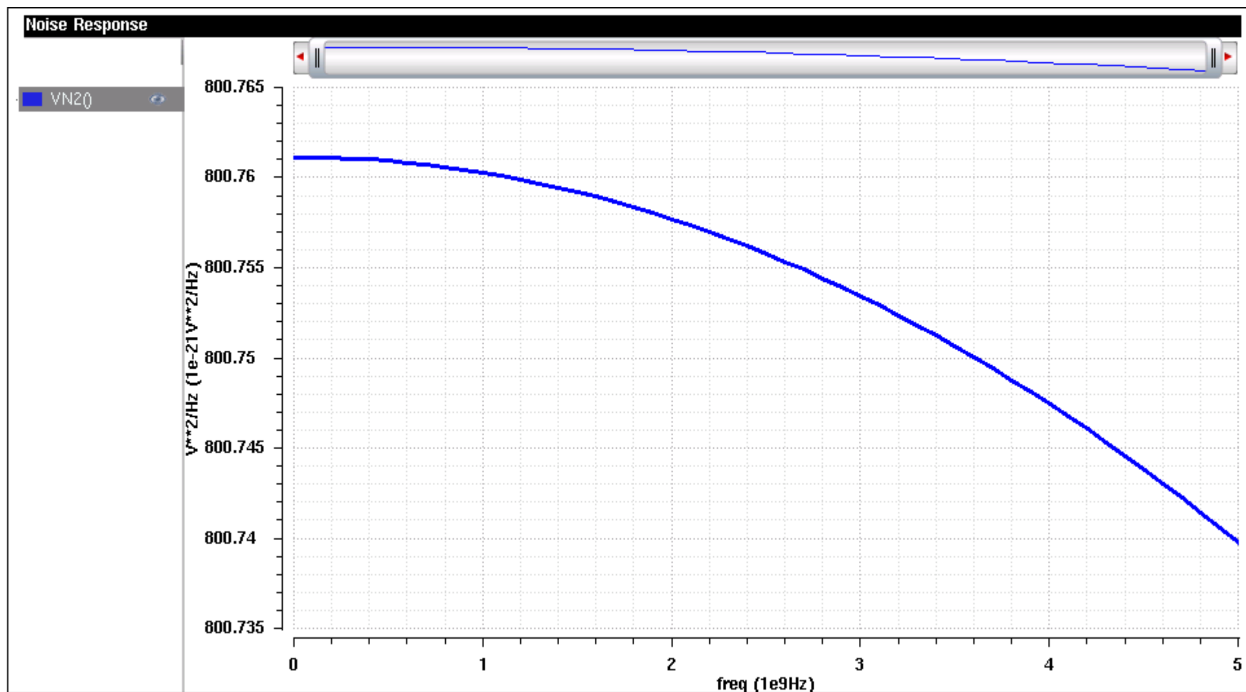

Fig.13. Noise response two CMOS gate @ 5 GHz.

With the increase in value of frequency the noise decreases. The average value of noise for two CMOS gate calculated is **800.8E-21.**

Reliability analysis is done in terms of delay vs. time. As it can be seen that the delay between input and output voltages increases as the circuit is analysed over prolonged time period [8].

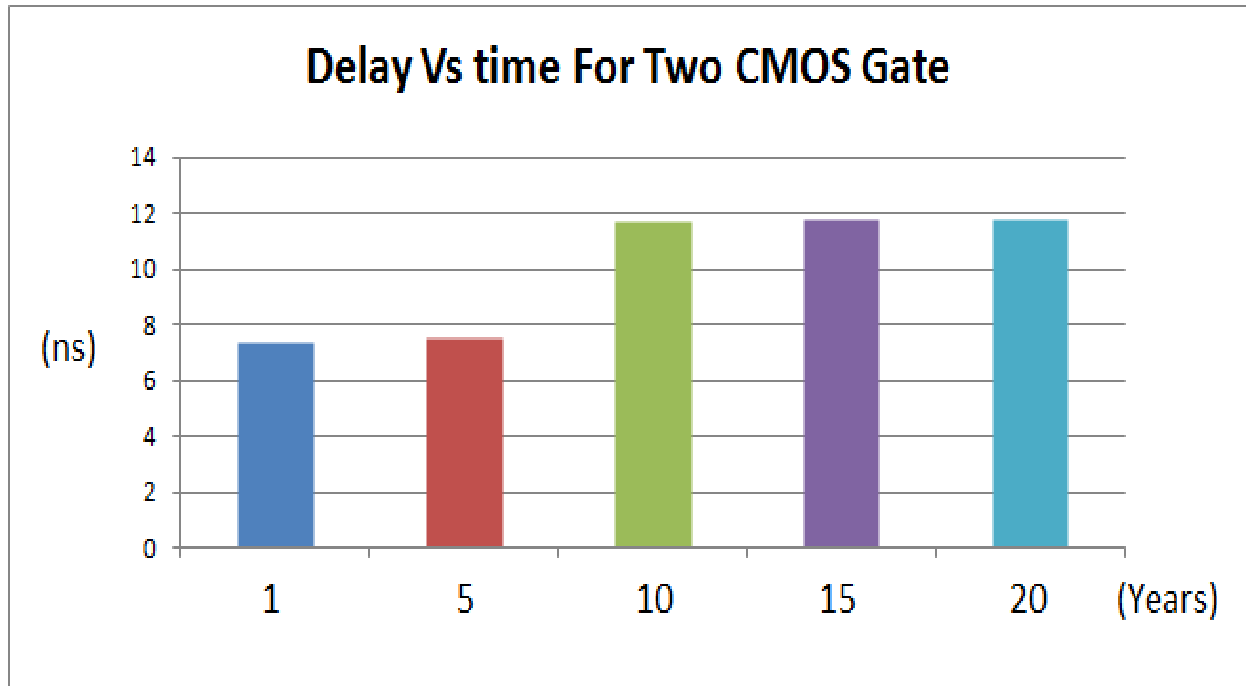

Fig.14. Reliability analysis in terms of delay vs. time for two CMOS gate.

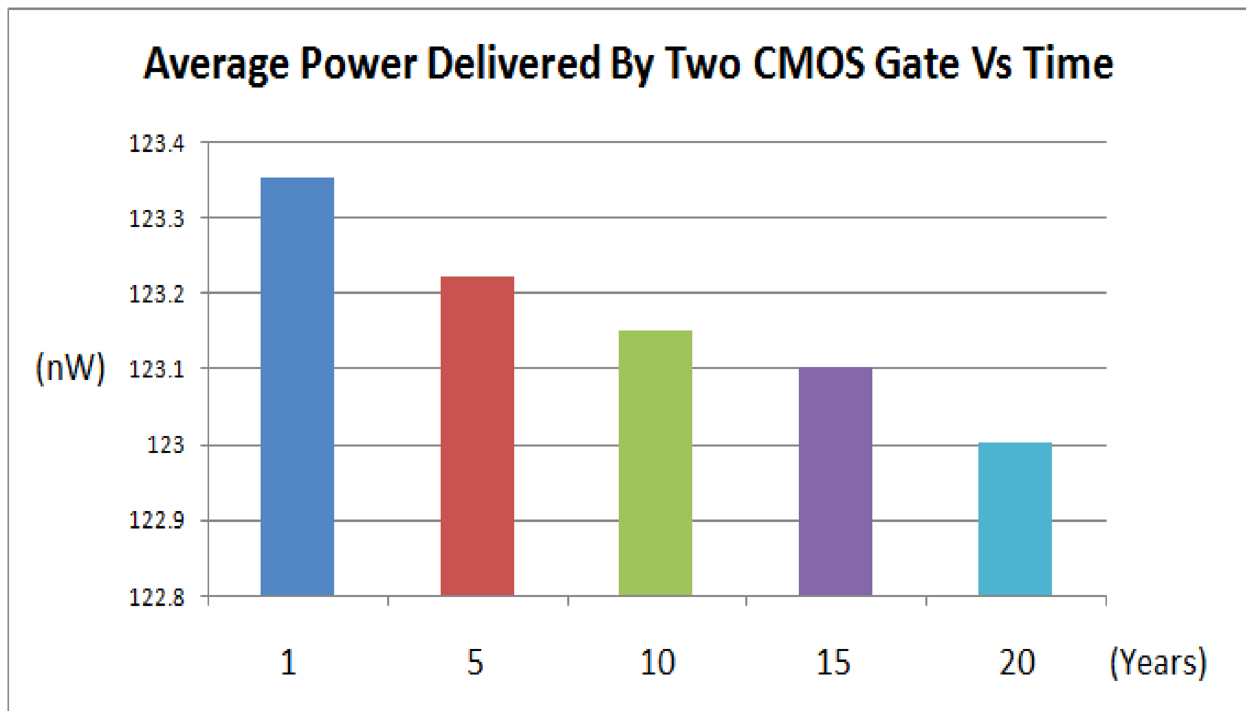

Fig.15. Reliability analysis in terms of average power delivered vs. time for two CMOS gate.

Conclusion: Thus the performance and reliability analysis of inverter and two CMOS gate is analyzed. It is noted that with the increase in time their performance degrades due to the effects of HCI, NBTI, PBTI and TDDB phenomenon. Reliability analysis for inverter is done only in terms of average power delivered by the circuit. Whereas the reliability analysis for two CMOS gate is done in terms of delay between input-output voltage and average power delivered by the circuit over different time intervals respectively. All the reliability simulation tools developed till yet are based on transistor level circuit simulation. So, taking into account higher level reliability simulator need to be developed, which take into account the factors such as switching activity, voltage overshoot and circuit sensitivity etc.

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